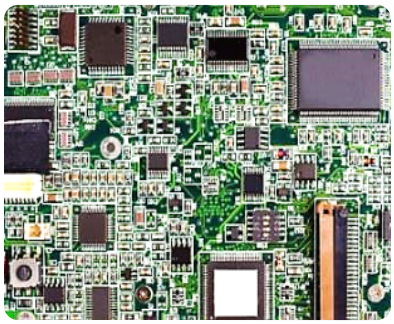
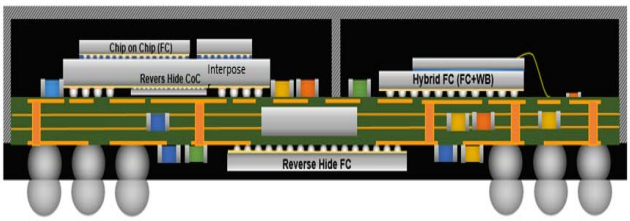
SIP : System in Package

Image



Reference Image



Description

SIP package containing combination of one or more multifunctional Ics with heterogeneous interconnection
Including passive components and MEMS/Sensor assembled into a single package EMI shielding with sputtering and plating.
Any combination of one or more integrated circuit(s) of different functionalities with various form and factors passive components and/or MEMS assembled into a single package.
Getting all or part of the functions of an electronic system on the standard PCB board for a moniturization
Achieving electrical/thermal performance enhancement purposes.

Application

- Power amplifiers, Antenna switches/Frontend module & transceiver, Connectivity module, MEMS integration with ASIC, Sensory module, automotive, 3G/4G model, Solid-state storage devices(SSD)

Feature

- Passive Component (≥ 01005)
- SAW,BAW filter, X-tal, Oscillator, Antenna
- EPS (Embedded Passive Substrate)
- EAD (Embedded Active Device)
- Core & Coreless Substrate
- Mold Grinding / Double Molding
- Shielding

Reliability

- MRT : JEDEC Level 3
- TC-B : -55˚C/125˚C, 1000 cycles
- HTS : 150˚C, 1000 hrs
- uHAST : 130˚C, 85% RH, 96 hrs

Bill of Materials and Process Specification

- PCB : BT or Equivalent (2~6 Layer)
- Adhesive : Paste or film
- Wire : Au (0.6~1.0 mil)
- EMC : Green
- Solder ball : Sn3.0Ag0.5Cu (Standard)
- Marking : Laser
- Packing : JEDEC Tray